



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-BAD/12/7484
Dated 19 Oct 2012

VIpower housed in SO-8: Assembly Process Changes

Table 1. Change Implementation Schedule

Forecasted implementation date for change	15-Jan-2013
Forecasted availability date of samples for customer	12-Oct-2012
Forecasted date for STMicroelectronics change Qualification Plan results availability	12-Oct-2012
Estimated date of changed product first shipment	18-Jan-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see list
Type of change	Package assembly material change
Reason for change	Products Rationalization
Description of the change	Progressing on the activities related to products rationalization, we are going to implement on VIPower products housed in SO-8 package some process changes: copper (Cu) wire bonding, new molding compound, high density lead-frame strip.
Change Product Identification	Finished-Good codes
Manufacturing Location(s)	1]St Shenzhen -China

DOCUMENT APPROVAL

Name	Function
Liporace, Nicola	Marketing Manager
Nicoloso, Riccardo	Product Manager
Minerva, Francesco	Q.A. Manager



VIPower housed in SO-8: Assembly Process Changes

WHAT:

Progressing on the activities related to products rationalization, we are going to implement on VIPower products housed in SO-8 package some process changes: copper (Cu) wire bonding, new molding compound, high density lead-frame strip.

See Below change matrix.

Item	Current	New
Molding Compound	NITTO MP8000CH4-2A	SUMITOMO EMEG700KC (Green resin)
Die Attach	QMI9507-2A1	QMI9507-2A1
Wires	Au 2 mils	Cu 2 mils
LeadFrame	uPPF std	uPPF High Density*
Lead-plating	Ni/Pd/Ag-Au	Ni/Pd/Ag-Au

*uPPF High Density =256 unit x strip (uFFP std= 120 units x strip)

WHY:

Products rationalization

HOW:

New configuration has been qualified as per attached report RR002112CT2235.
Samples available on customer's request through our Sales offices.

WHEN:

We plan to start production with new SO-8 configuration from January 2013 onward.

Package SO8 assembly process changes qualification
High Density Frame, Copper wires, Molding Compound

General Informations test vehicle 1	
Product Line	VNQ9
Commercial Product	VN5E160S-E
Silicon process technology	M05E
Package	SO8

Locations	
Diffusion fab location	ST CT6 Catania (Italy)
Assembly plant location	ST Shenzhen (China)
Test plant location	ST Shenzhen (China)
Reliability lab location	ST Catania (Italy)

General Informations test vehicle 2	
Product Line	VNY7
Commercial Product	VNL5030S5-E
Silicon process technology	M05
Package	SO8

Locations	
Diffusion fab location	ST AMK6 Ang Mo Kio (Singapore)
Assembly plant location	ST Shenzhen (China)
Test plant location	ST Shenzhen (China)
Reliability lab location	ST Catania (Italy)

General Informations test vehicle 3	
Product Line	VNL6
Commercial Product	VNS1NV04P-E
Silicon process technology	M03.5
Package	SO8

Locations	
Diffusion fab location	ST AMK6 Ang Mo Kio (Singapore)
Assembly plant location	ST Shenzhen (China)
Test plant location	ST Shenzhen (China)
Reliability lab location	ST Catania (Italy)

Author:
 F.CERAULO
 Product Qualification Eng
 APG Q&R Catania

Reliability and electrical test executed by:
 M. Palermo
 Rel. Eng.
 IMS Rel Dept. – APG Support

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- 1. Reliability evaluations overview

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on several test vehicles in order to qualify some process changes involves the SO8 package in ST Shenzhen:

- 1) Frame migration from Std to High Density
- 2) Copper 2.0 mils wires usage
- 3) New molding compound

The chosen test vehicles are: **VN5E160S-E** (VNQ9 as ST internal code) that is a high side driver designed in VIPower M05E technology, the **VNL5030S5-E** (VNY7 as ST internal code) that is an Omnifet III fully protected low side driver designed in VIPower M05 technology, the **VNS1NV04P-E** (VNL6 as ST internal code) that is an Omnifet II fully autoprotected Power MOSFET designed in VIPower M03.5 technology.

The qualification was based on 3 lots, one lot per vehicle, according to the **AEC_Q100 Rev.G** specification for the Accelerated Environment Stress (test Group A) and the Accelerated Lifetime Simulation (test Group B) the following tests were performed on each lot: Temperature Humidity Bias (THB), Thermal Cycling (TC), High Temperature Storage (HTS) and Environmental Sequence (ES). Only the **VNL5030S5-E** as max die size for the chosen test vehicles was submitted also to the High Temperature Operative Life (HTOL) test on 3 lots and to the Power Temperature Cycling (PTC) on 1 lot.

The Package Assembly Integrity (test Group C) verifications including Wire Bond Pull/Shear tests (WBP, WBS), Physical Dimension (PD) and Solderability (SD) didn't pointed out neither abnormal break loads nor forbidden failure modes.

1.2 Results

All reliability tests have been completed with positive results, neither functional nor parametric rejects were detected at final electrical testing.

The Device Physical Analysis (DPA) performed on stressed units including the Wire Bond Pull/Shear tests (WBP, WBS) as Package Assembly Integrity (test Group C) didn't pointed out neither abnormal break loads nor forbidden failure modes.

Based on the overall positive results we consider the products assembled with the new frame qualified from a reliability point of view.

- 2. Traceability

VN5E160S-E (VNQ9)

Wafer fab information	
Wafer fab manufacturing location	ST CT 6" CATANIA (Italy)
Wafer diameter	6
Silicon process technology	VIPOWER M0_A5
Die finishing back side	Ti-Ni-Au
Die size	1340 x 2330 micron
Metal materials/levels	Ti/TiN/Ti/AISiCu 3.2 micron/ 2 level
Passivation	SiN / Polyimide
Lot #	3142872

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package description	SO 8L 169x92 Mtx HD OpK NiThPdAgAu
Molding compound	RESIN SUMITOMO EME-G700KC
Wires bonding materials/diameters	Cu 2.0 mils
Die attach material	LOCTITE – QMI9507-2A1
Assy Lots #	GK20500H05

Final Testing Information	
Electrical testing manufacturing location	ST Shenzhen (China)

VNL5030S5-E (VNY7)

Wafer fab information	
Wafer fab manufacturing location	ST AMK6 Ang Mo Kio (Singapore)
Wafer diameter	6
Silicon process technology	VIPOWER M0_5
Die finishing back side	Ti-Ni-Au
Die size	3180 x 1890
Metal materials/levels	2 levels / Ti/TiN/Ti/AICu (3.2 µm last level)
Passivation	SiN / Polyimide
Lot #	Lot 1: 62037Y1, Lot 2: 6204E1T, Lot 3: 6205KE2

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package description	SO 8L 169x92 Mtx HD OpK
Molding compound	RESIN SUMITOMO EME-G700KC
Wires bonding materials/diameters	Cu 2.0mils
Die attach material	GLUE QMI9507-2A1 10cc/41g
Assy Lots #	Lot1: GK2120UQ01, Lot2: GK2120UU01, Lot3: GK2120UT01

Final Testing Information	
Electrical testing manufacturing location	ST Shenzhen (China)

VNS1NV04P-E (VNL6)

Wafer fab information	
Wafer fab manufacturing location	ST AMK 6" Ang Mo Kio (Singapore)
Wafer diameter	6
Silicon process technology	VIPOWER M0_A3
Die finishing back side	Ti-Ni-Au
Die size	1710 x 1520 micron
Metal materials/levels	AlSi (3.2 micron) / 1
Passivation	SiN / Polyimide
Lot #	61395Y2

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package description	SO 8L 2x81x109 MtHD OpJ NiThPdAgAu
Molding compound	RESIN SUMITOMO EME-G700KC
Wires bonding materials/diameters	Cu 2.0 mils
Die attach material	LOCTITE – QMI9507-2A1
Assy Lots #	GK2050VL01

Final Testing Information	
Electrical testing manufacturing location	ST Shenzhen (China)

- 3. VN5E160S-E - Devices characteristics

3.1 Generalities



VN5E160S-E

Single channel high side driver for automotive applications

Features

Max transient supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 28V
Max On-state resistance (per ch.)	R_{ON}	160 m Ω
Current limitation (typ)	I_{LIMH}	10A
Off state supply current	I_S	2 μ A ⁽¹⁾

1. Typical value with all loads connected.

■ General

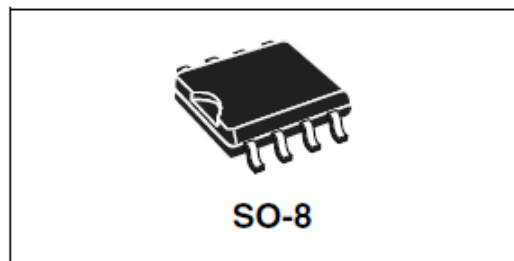
- Inrush current active management by power limitation
- Very low stand-by current
- 3.0V CMOS compatible inputs
- Optimized electromagnetic emissions
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC european directive

■ Diagnostic functions

- Open Drain status output
- On-state open load detection
- Off-state open load detection
- Output short to V_{CC} detection
- Overload and short to ground (power limitation) indication
- Thermal shutdown indication

■ Protections

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Over-temperature shutdown with autorestart (thermal shutdown)
- Reverse battery protected ^(a)
- Electrostatic discharge protection



Application

- All types of resistive, inductive and capacitive loads

Description

The VN5E160S-E is a single channel high-side driver manufactured in the ST proprietary VIPower M0-5 technology and housed in the tiny SO-8 package.

The VN5E160S-E is designed to drive automotive grounded loads delivering protection, diagnostics and easy 3V and 5V CMOS-compatible interface with any microcontroller.

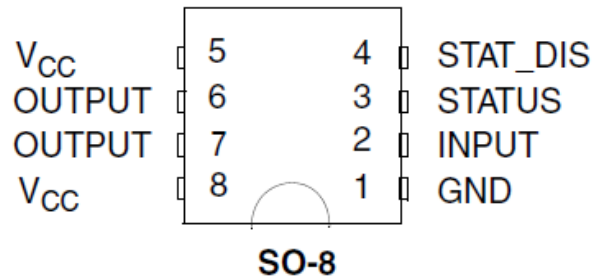
The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, over-temperature shut-off with auto-restart and over-voltage active clamp.

A dedicated active low digital status pin is associated with every output channel in order to provide *Enhanced* diagnostic functions including fast detection of overload and short-circuit to ground, over-temperature indication, short-circuit to V_{CC} diagnosis and ON & OFF state open-load detection.

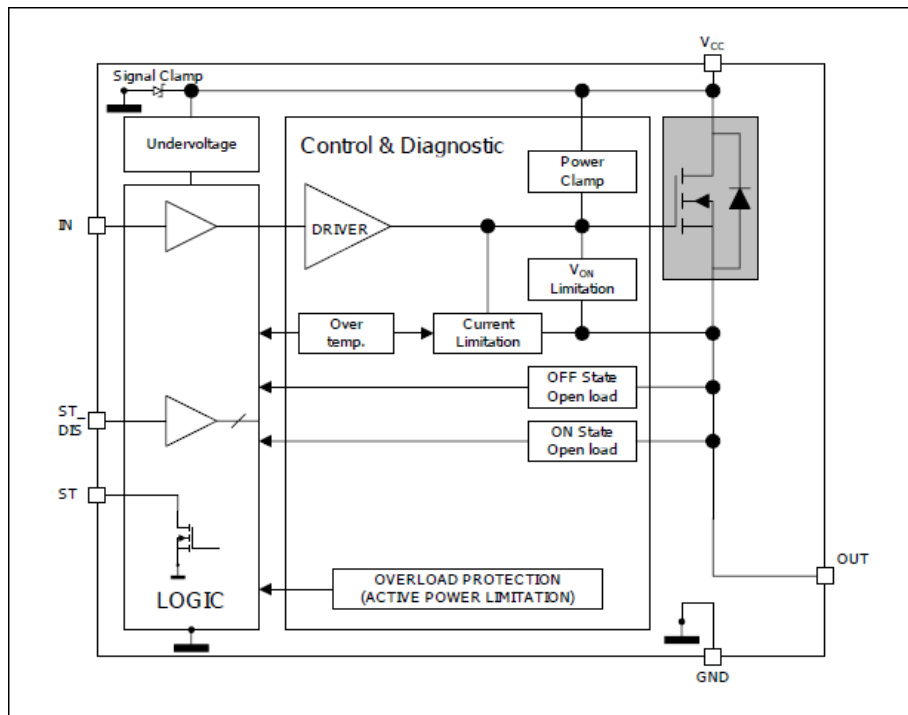
The diagnostic feedback of the whole device can be disabled by pulling the STAT_DIS pin up, thus allowing wired-ORing with other similar devices.

a. See [Figure 32: Application schematic](#).

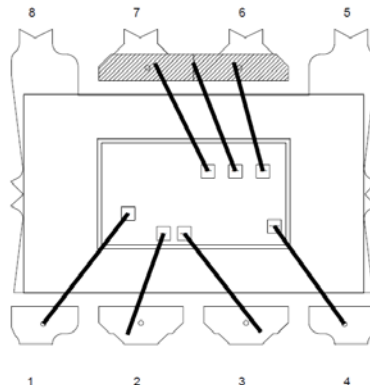
3.2 Pins connection



3.3 Blocks diagram



3.4 Bonding diagram



- 4. VNL5030S5-E - Devices characteristics

4.1 Generalities



VNL5030J-E VNL5030S5-E

OMNIFET III
fully protected low-side driver

Target specification

Features

Type	V _{clamp}	R _{DS(on)}	I _D
VNL5030J-E	41 V	30 mΩ	25 A
VNL5030S5-E			

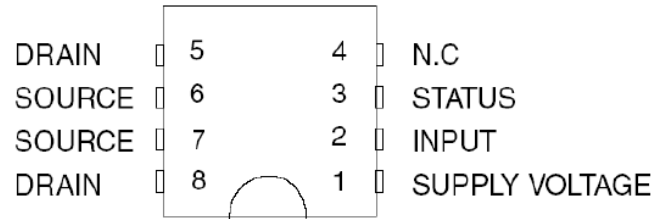
- Drain current: 25 A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC european directive
- Open drain status output



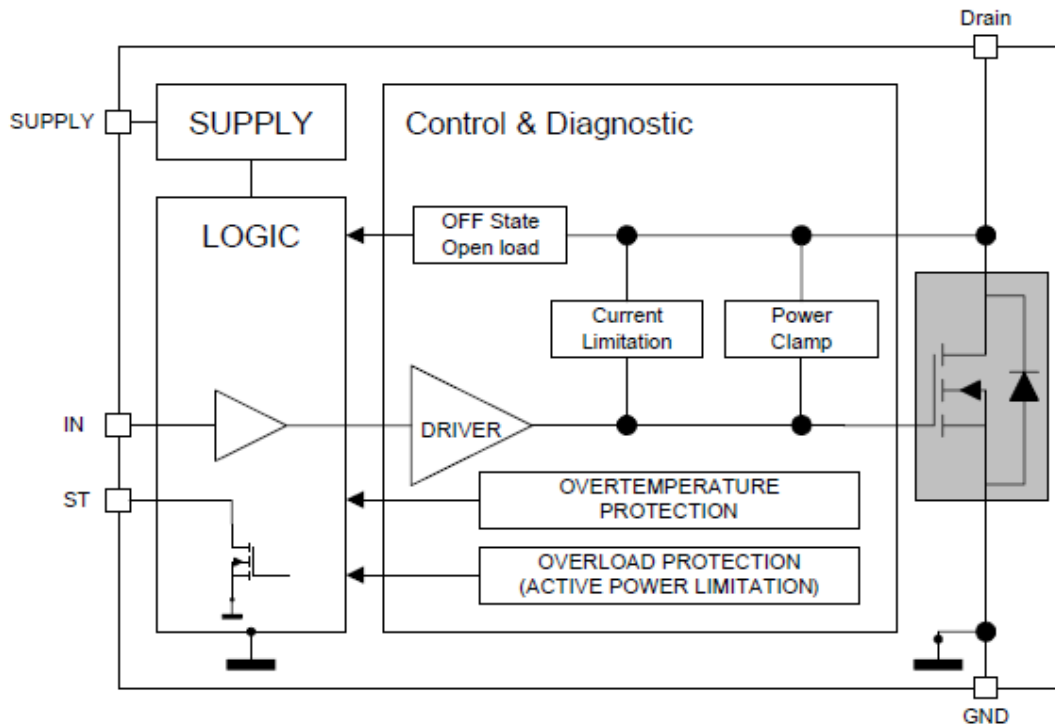
Description

The VNL5030J-E and VNL5030S5-E are monolithic devices made using STMicroelectronics™ VIPower™ technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. Output current limitation protects the devices in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

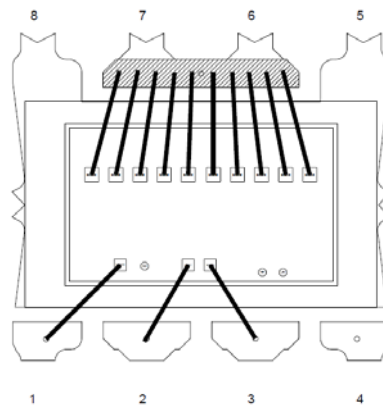
4.2 Pins connection



4.3 Blocks diagram



3.4 Bonding diagram



- 5. VNS1NV04P-E - Devices characteristics

5.1 Generalities



VNN1NV04P-E, VNS1NV04P-E

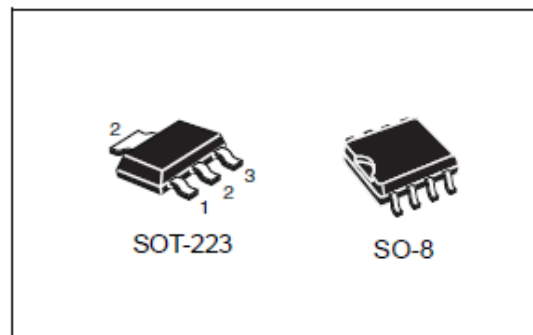
OMNIFET II

fully autoprotected Power MOSFET

Features

Parameter	Symbol	Value
Max on-state resistance (per ch.)	R_{ON}	250 m Ω
Current limitation (typ)	I_{LIMH}	1.7 A
Drain-source clamp voltage	V_{CLAMP}	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



Description

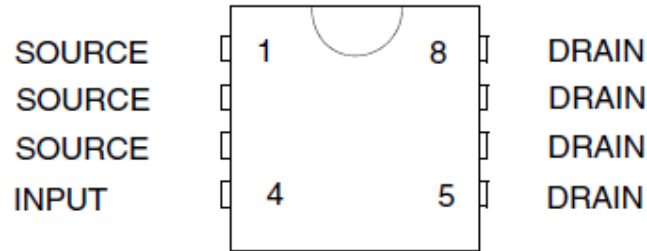
The VNN1NV04P-E, VNS1NV04P-E are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

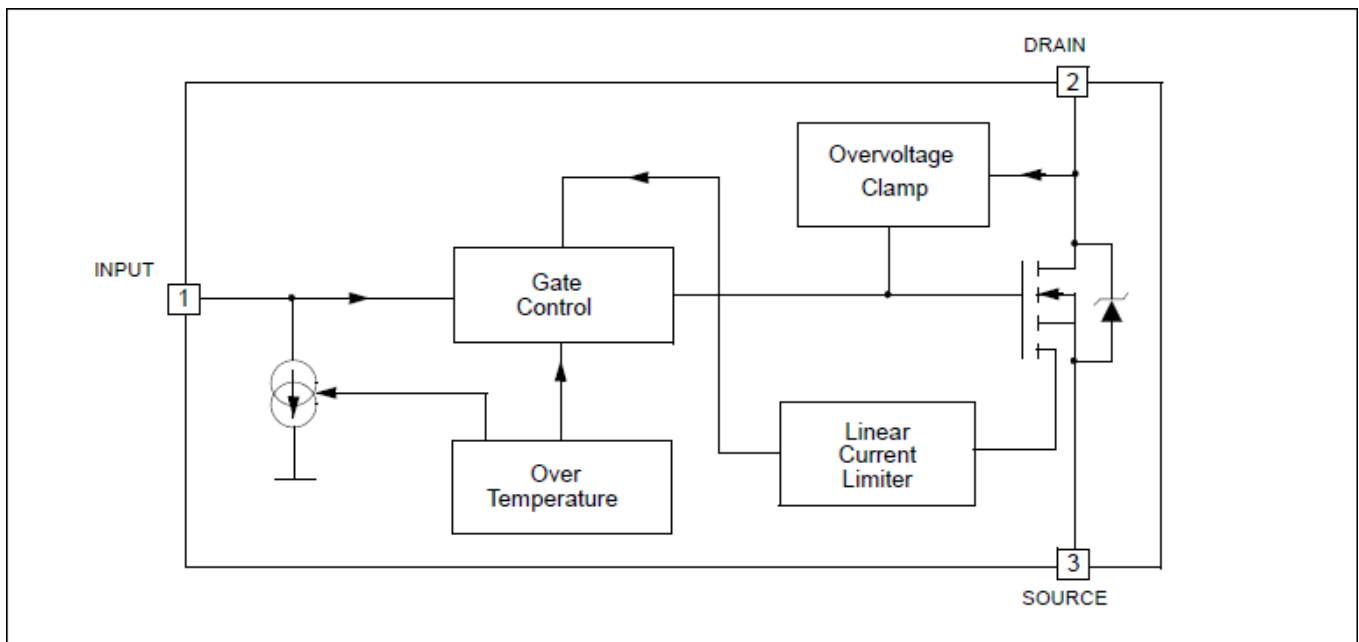
Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SOT-223	VNN1NV04P-E	VNN1NV04PTR-E
SO-8	VNS1NV04P-E	VNS1NV04PTR-E

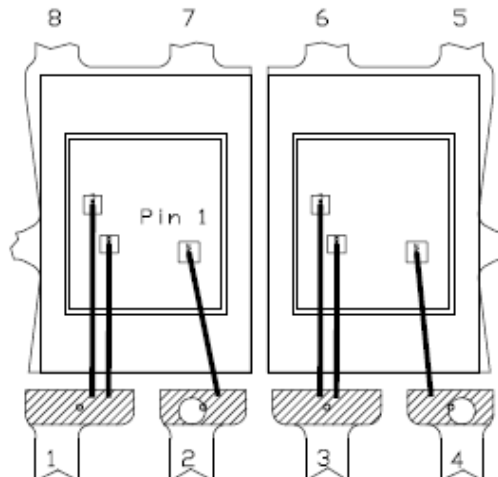
5.2 Pins connection



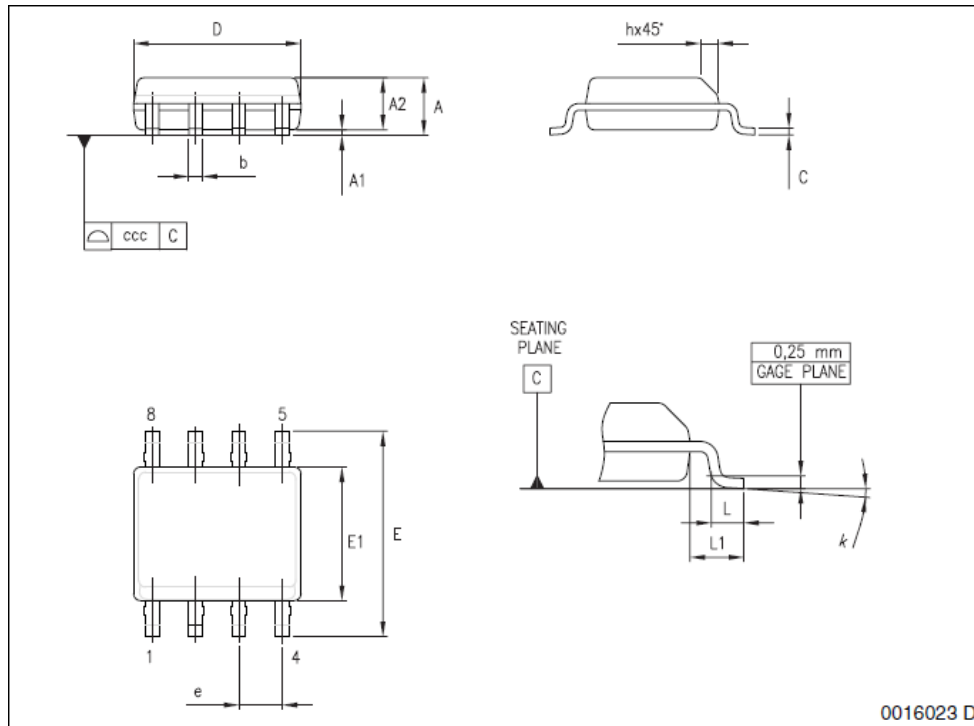
5.3 Blocks diagram



5.4 Bonding diagram



- 6. Package outline/Mechanical data



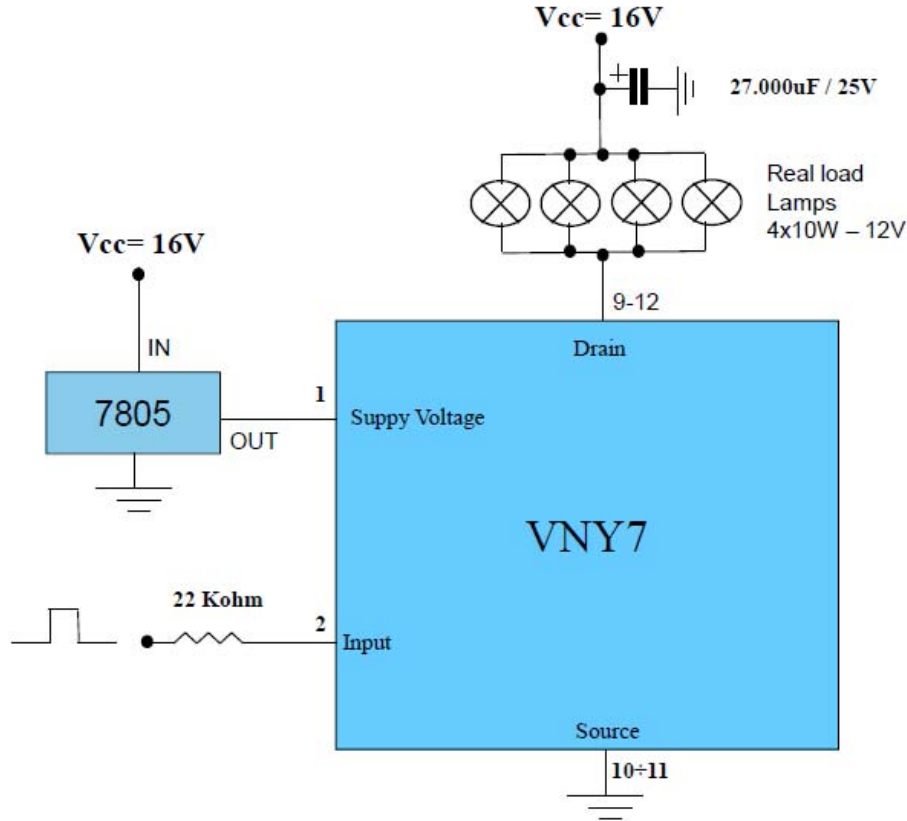
Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

- 7. Reliability qualification plan and results

AEC #	Test Name	STM Test Conditions	Sample Size/Lots	Results Fails/SS/Lots	Comments
A1	PC Pre Cond	- Preconditioning according to level 3 Jedec JESD22-A113F - Reflow according to Jedec JSTD020D-1	Before THB, ES, TC. Reliability executed on units soldered on PCB		
A2	THB Temp Humidity Bias	Ta=85°C, RH=85%, Vcc=24V for 1000 hours	77/3	0/77/3	1 lot each test vehicle
A3	ES Environmental Sequence	TC (Ta=-65°C / +150°C for 100 cycles) + AC (Ta=121°C, Pa=2atm for 96 hours)	77/3	0/77/3	1 lot each test vehicle
A4	TC Temp. Cycling	Ta=-65°C / +150°C for 500 cycles	77/3	0/77/3	1 lot each test vehicle
A5	PTC Power Temp. Cycling	Per JA105. Ta=-40°C / +125°C for 1000 cycles. Test before and after at room and hot temperatures.	45/1	0/45/1	Only on VNL5030S5-E Incandescent lamps loads 4x10W, Ton=10ms, Toff=30s, 120K activations within 1000cy
A6	HTSL High Temp. Storage Life	Ta=150°C for 1000 hours. TST before and after at room and hot temperatures.	77/3	0/77/3	1 lot each test vehicle
B1	HTOL High Temp. Op. Life	Bias Static stress (JESD22-A108): Ta=125°C, Vcc=30V for 1000 hours	77/3	0/77/3	Only on VNL5030S5-E
C1	WBS Wire Bond Shear	Per AEC-Q100-001	30 bonds from minimum 5 of units from 1 lot	Passed	
C2	WBP Wire Bond Pull	Per MIL-STD883, M2011	30 bonds from minimum 5 of units from 1 lot	Passed	
C3	SD Solderability	JESD22-B102	15/1	Passed	
C4	PD Physical Dimensions	Per case outline. See applicable JEDEC standard outline and individual device spec for significant dimensions and tolerances.	30/1	Passed	
E8	GL Gate Leakage		6/1	Passed	

- 8. PTC (resistive) schematics

PTC test configuration, $T_a = -40^{\circ}\text{C} / +125^{\circ}\text{C}$



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